Microelectronics
Exercises of Topic 5

ICT Systems Engineering
EPSEM - UPC

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5 Analog integrated circuits

EXERCISE 5.1 This problem aims to follow the steps in the design of a MOS transistor amplifier that provides a voltage amplification $|A_v| = |v_o/v_i| = 10$.

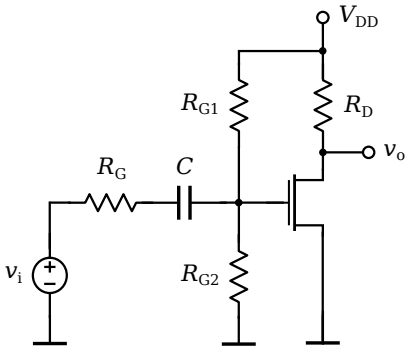

Figure 1

For the circuit in Figure 1, knowing that $V_{DD} = 5$ V, $R_G = R_D = 1$ kΩ, $K' = 20$ μA/V^2, $V_T = 1$ V and that C is large, so that it may be considered a shortcircuit except for the bias circuit:

a) Draw the corresponding bias and small-signal analysis circuits.

b) Find the drain current at the operating point of the transistor, I_{DQ}, imposing that the output voltage v_o at this point is half times the supply voltage (this guarantees the maximum dynamic range at the output, i.e., the maximum distance of the operating point to the limits imposed by ground and V_{DD}).

c) Obtain the voltage amplification of the circuit $|A_v| = |v_o/v_i|$ as a function of the transconductance of the transistor g_m. Assuming that the desired amplification is $|A_v| = 10$, determine g_m and, from it, the aspect ratio of the transistor W/L.

d) Find the gate-source voltage at the operating point V_{GSQ} and, from the obtained result, propose appropriate values for R_{G1} and R_{G2}.

e) Finally, provide the complete mathematical expression of the output voltage v_o.

EXERCISE 5.2 The goal of this problem is to redesign the circuit presented in the previous exercise (Figure 1) to replace the resistors by MOS transistors, thereby saving integration area. Assume that the minimum-size transistor available with the technology used has $W = 3$ µm and $L = 2$ µm.

a) Design a PMOS active load ($K'_P = 10$ µA/V^2, $V_T = -1$ V) to substitute the resistor R_D. Specifically, the active load must exhibit a small-signal resistance equal to 1 kΩ, and it must also provide an output voltage at the operating point that halves that of the supply. Note that for the operating point the active load behaves like a nonlinear resistance, characterized by the equation of the MOS transistor in saturation, whereas for small signal it behaves like a linear resistor controlled by the transconductance of the transistor.

b) Find the new value of the NMOS transistor current at the operating point, I_{DQ}.

c) Determine the new dimensions of the NMOS transistor to achieve $|A_v| = |v_o/v_i| = 10$.

d) Determine the gate-source voltage of the NMOS transistor at the operating point, V_{GSQ}, and from it, design a CMOS bias network to replace R_{G1} and R_{G2} (impose that the current drawn by this network equals 10 µA).

e) Draw the complete circuit schematic of the final design.

EXERCISE 5.3 This problem aims to follow the steps in the design of a bipolar transistor amplifier.

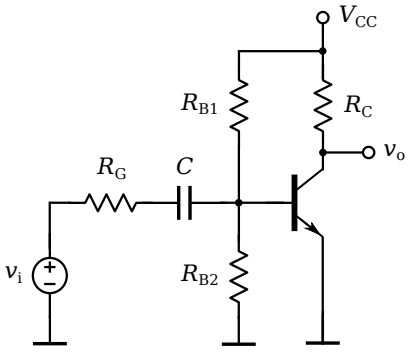

Figure 2

For the circuit in Figure 2, knowing that $V_{CC} = 5$ V, $R_G = 10$ Ω, $R_C = 1$ kΩ, $V_T = 25$ mV, $V_\gamma = 0.7$ V, $\beta = 100$ and that C is large, so that it may be considered a shortcircuit except for the bias circuit:

a) Draw the corresponding bias and small-signal analysis circuits.

b) Calculate the collector current at the operating point of the transistor, I_{CQ}, imposing that the output voltage v_o at this point is half times the supply voltage (this guarantees the maximum dynamic range at the output, i.e., the maximum distance of the operating point to the limits imposed by ground and V_{CC}).

c) Calculate the voltage amplification of the circuit, $A_v = |v_o/v_i|$, as a function of the transconductance of the transistor g_m. Prove that under the criterion applied in the previous question, the resulting amplification is $A_v = |v_o/v_i| = 20V_{CC} = 100$.

d) Taking into account that the transistor is in the conduction region and, therefore, it can be assumed that $v_{BE} \approx V\gamma$, find the base current at the operating point, I_{BQ}, and from this result propose appropriate values for R_{B1} and R_{B2}.

e) Finally, provide the complete mathematical expression of the output voltage v_o.

EXERCISE 5.4 For the amplifier with active load in Figure 3,

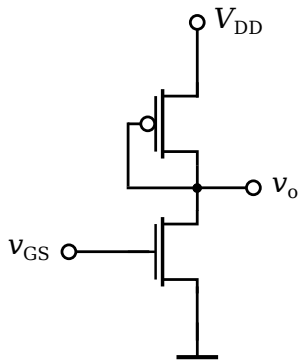

Figure 3

and knowing that $V_{DD} = 3$ V, $K'_P = 10$ μA/V^2, $K'_N = 20$ μA/V^2, $V_{TP} = -0.5$ V and $V_{TN} = 0.5$ V:

a) Design the PMOS active load so that the output voltage at the operating point is half times that of the supply, and so that the small-signal resistance equals 1 kΩ.

b) Find the dimensions of the NMOS transistor to achieve a small-signal voltage amplification $|A_v| = 5$.

c) Determine the value of the input voltage at the operating point, V_{GSQ}, necessary to achieve the desired performance.

EXERCISE 5.5 Figure 4 shows the schematic of a current mirror, a circuit commonly used in microelectronic design to set the current i_2 that flows through a given subcircuit from the current i_1 absorbed by the transistor M_1.

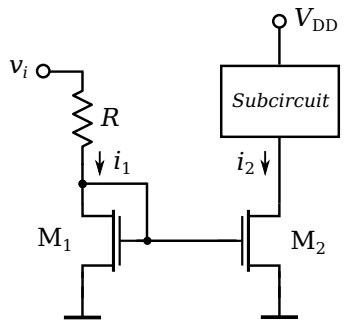

Figure 4

a) Demonstrate that if both transistors are identical and operate in saturation mode the currents i_1 and i_2 must necessarily be equal (hence the name of current mirror). This property ideally applies at low frequency when the capacitances of the transistors and other parasitic effects can be ignored.

b) Find the gain of the mirror, i.e., i_2/i_1, when the transistors exhibit different dimensions.

c) Knowing that $R = 10$ kΩ, $K' = 20$ μA/V^2, $V_T = 0.5$ V, that the technology allows $L_{min} = 1.8$ μm, $W_{min} = 2.4$ μm and that $v_i = V_{DD} = 5$ V, find the minimum dimensions of the transistors required to achieve $i_2 = 10$ mA.

EXERCISE 5.6 Figure 5 shows the schematic of an NMOS transistor amplifier.

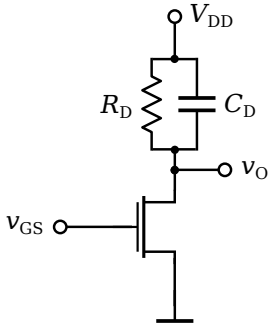

Figure 5

The supply voltage is $V_{DD} = 1.5$ V and the devices exhibit the following features:

- Transistor: $K' = 20$ μA/V^2, $V_T = 0.5$ V, $W = 14.94$ μm, $L = 0.18$ μm.
- Resistor: N well with sheet resistance $R_s = 4$ kΩ/square, $W = 0.24$ μm, $L = 0.6$ μm.
- Capacitor: Metal 1-Metal 2 structure with specific capacitance $C_s = 1$ fF/μm^2.

It is requested:

a) Knowing that the operating point of the voltage at the input of the transistor is $V_{GSQ} = 0.8\,\mathrm{V}$, find the corresponding drain bias current, I_{DQ}.

b) Calculate the small-signal amplification of the circuit at low and at high frequencies. In view of the results, what kind of filtering does the amplifier perform?

c) Design the capacitor so that the -3-dB cut-off frequency equals 8 MHz.

EXERCISE 5.7 The CMOS inverter is a basic component in digital circuits, where signals take two discrete levels. The inverter, however, also has other applications, e.g., an analog amplifier. Consider the CMOS inverter having the transfer characteristic shown in Figure 6.

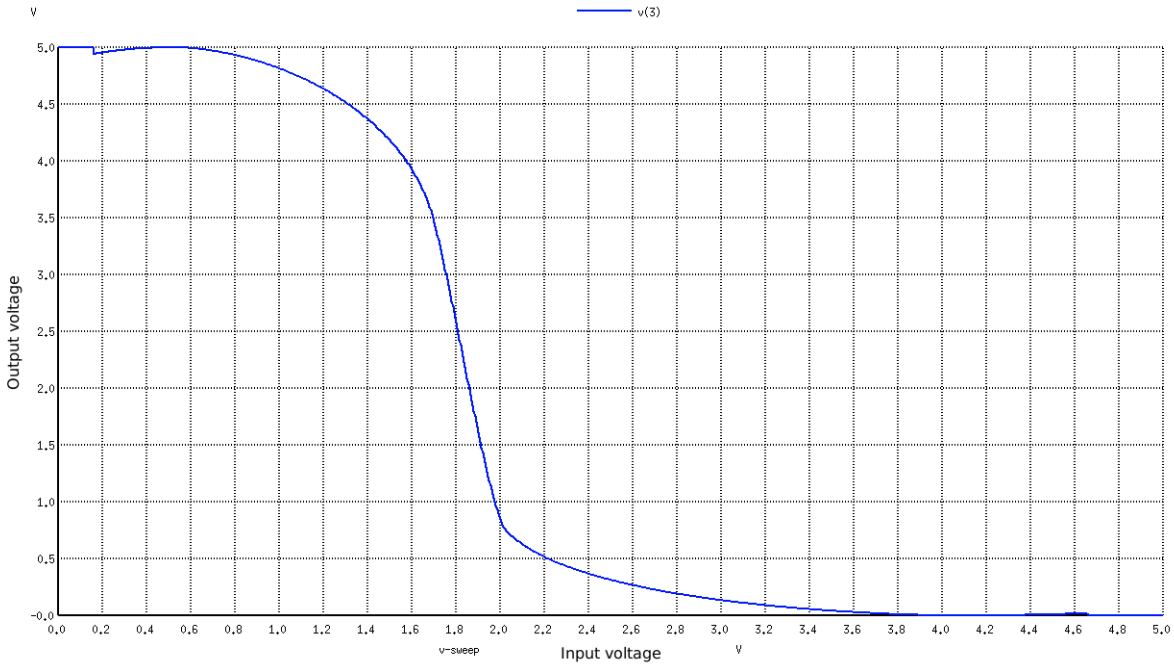

Figure 6

Assume that you want to use this inverter to amplify a low-frequency sinusoidal signal coming from a voltage source v_g exhibiting an amplitude of 100 mV.

a) Explain what needs to be done in order to properly amplify this signal with the CMOS inverter.

b) Give the schematic of a suitable circuit that, making use of the aforementioned inverter and other elements that provide suitable coupling of the signal v_g, achieves the desired function.

c) Determine the output amplitude, as well as the amplification provided by the circuit.